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10/799,628	03/15/2004	Manabu Sasaki	520.43638X00	8414

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EXAMINER	
SHEN, KEZHEN	

ART UNIT	PAPER NUMBER
2609	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/799,628	SASAKI, MANABU	
	Examiner	Art Unit	
	Kezhen Shen	2609	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-6 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-6 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sako et al. (US 6853613 B1) in view of Nagase et al. (US 2003/0140207 A1) and Kamiya et al. (5,109,498).

Regarding claim 1 Sako et al. teaches an optical disk drive apparatus (40 of Fig. 8), for reading-out information from an optical disk (1 of Fig. 8), having a plural number of information recording layers made up in a direction of rotation axis thereof (Col 6 Line 47-50 the first and second recording layer are axis coincidence relative to each other), through irradiating a light beam upon the information recording layer (Col 7 Line 12-16 the light beam radiated on the first or second recording layer), and for transferring the

information read out to a host-computer, responding to a transfer request from said host-computer (Col 7 Line 36-41 The control signal from the controller may be from a personal computer), comprising of a memory configured to memorize the information read out from said information recording layers (43 and 46 of Fig. 8, Col 7 Line 43-44 data from the first and second recording layers are stored in the buffer memories) and a processor configured to control said memory (Col 7 Line 34-38 The CPU or controller [47 of Fig. 8] is provided with plural of operating switches including the buffer management unit [46 of Fig. 8], Col 8 Line 3-6 The first and second buffer memory is controlled and supervised by the buffer management unit [46 of Fig. 8]), wherein said processor supervises accesses to each of said plural number of the information recording layers, and memorizes information which follows information, upon which a transfer request is made from said host-computer, into a predetermined area of said memory, upon basis of a frequency of the accesses obtained through the supervision thereof.

Sako et al. fails to teach said processor supervises accesses to each of said plural number of the information recording layers, and memorizes information which follows information, upon which a transfer request is made from said host-computer, into a predetermined area of said memory, upon basis of a frequency of the accesses obtained through the supervision thereof; however, Nagase et al. and Kamiya et al. describes such a system. Kamiya et al. teaches the buffer memory to have a plurality of cache areas each of which has a predetermined area size which intercedes between the processor and memory (Kamiya et al. Col 2 Line 12-14 a buffer memory device

comprise a cache memory having a plurality of cache areas each of which has a predetermined area size). Nagase et al. teaches a system of reducing an access time to storage areas by maintaining a table of number of accesses made to the data block frequency of access to a memory (Nagase et al. [0034] the controller also includes an access table maintaining records of number of access made to data blocks in the storage area over a given period of time).

Therefore, the combined teaching of Kamiya et al. and Nagase et al. in view of Sako et al. would have rendered obvious a the processor transferring information between host-computer and predetermined area of said memory as claimed for the benefit of faster access time between the memory buffer and processor.

Regarding claim 2 Sako et al. fails to teach teaches the optical disk drive apparatus, as described in the claim 1, wherein said memory comprises said predetermined areas in a plural number thereof, being equal to or greater than two (2). However, Kaymiya et al. teaches a memory buffer having a plurality of cache areas each of which has a predetermined area size (Kaymiya et al. Col 2 Line 6-14).

Therefore, the teaching of Kamiya et al. in view of Sako et al. would have rendered obvious the memory having a plural number of predetermined areas for the benefit of effectively using the cache memory for memorizing the instruction and data signals.

Regarding claim 3 Sako et al. fails to teach the optical disk drive apparatus, as described in the claim 1, wherein said processor further makes management on the access frequency for each of information recorded in each layer of said optical disk,

from which the information is read out. However, Nagase et al. teaches a table for number of accesses made to data blocks in the storage area managed by the controller (Nagase et al. [0034] and [0035]) and Sako et al. teaches individual recording layers which are inherently two different storage areas.

Therefore, the teaching of Nagase et al. in view of Sako et al. would have rendered obvious the management of access frequency for the information recorded in each of the recording layers on the optical disk for the benefit of efficiently managing the data blocks of each layer.

Regarding claim 4 Sako et al. teaches a method for reproducing data, comprising, the following steps of reading out information from an information recording layer, by irradiating a light beam upon an optical disk having a plural number of the information recording layers (Col 7 Line 12-16 the light beam radiated on the first or second recording layer), being piled up in a direction of rotation axis thereof (Col 6 Line 47-50 the first and second recording layer are axis coincidence relative to each other), in accordance with a transfer request from a host-computer (Col 7 Line 36-41 The control signal from the controller may be from a personal computer), memorizing the information read out form said information recording layer into a memory (Col 7 Line 43-44 data from the first and second recording layers are stored in the buffer memories [43 and 46 of Fig. 8]), transferring the information memorized in said memory to said host-computer (Col 9 Line 17-21 The data from the buffer memories are output at an output terminal [51 of Fig. 8]) and supervising an access to an each layer of said plural number of the information recording layers, and memorizing information, which follows

information, upon which the transfer request is made from said host-computer, into a predetermined area of said memory, upon basis of a frequency of the accesses obtained through the supervision thereof.

Sako et al. fails to teach said processor supervises accesses to each of said plural number of the information recording layers, and memorizes information which follows information, upon which a transfer request is made from said host-computer, into a predetermined area of said memory, upon basis of a frequency of the accesses obtained through the supervision thereof, however Nagase et al. and Kamiya et al. describes such a system. Kamiya et al. teaches the buffer memory to have a plurality of cache areas each of which has a predetermined area size which intercedes between the processor and memory (Col 2 Line 12-14 a buffer memory device comprise a cache memory having a plurality of cache areas each of which has a predetermined area size). Nagase et al. teaches a system of reducing an access time to storage areas by maintaining a table of number of accesses made to the data block frequency of access to a memory ([0034] the controller also includes an access table maintaining records of number of access made to data blocks in the storage area over a given period of time).

Therefore, the combined teaching of Kamiya et al. and Uehigashi in view of Sako et al. would have rendered obvious a the processor transferring information between host-computer and predetermined area of said memory as claimed for the benefit of faster access time between the memory buffer and processor.

Regarding claim 5 Sako et al. teaches the method for reproducing data, as described in the claim 4, wherein said memory comprises said predetermined areas in a plural number thereof, being equal to or greater than two (2).

However, Kaymiya et al. teaches a memory buffer having a plurality of cache areas each of which has a predetermined area size (Kaymiya et al. Col 2 Line 6-14). Therefore, the teaching of Kamiya et al. in view of Sako et al. would have rendered obvious the memory having a plural number of predetermined areas for the benefit of effectively using the cache memory for memorizing the instruction and data signals.

Regarding claim 6 Sako et al. fails to teach the method for reproducing data, as described in the claim 4, wherein the supervision on the access frequency is made for an each layer of those layers of said optical disk, from which the information is read out. However, Nagase et al. teaches a table for number of accesses made to data blocks in the storage area managed by the controller (Nagase et al. [0034] and [0035]) and Sako et al. teaches individual recording layers which are inherently two different storage areas.

Therefore, the teaching of Nagase et al. in view of Sako et al. would have rendered obvious the management of access frequency for the information recorded in each of the recording layers on the optical disk for the benefit of efficiently managing the data blocks of each layer.

Examiner's Note

The referenced citations made in the rejection(s) above are intended to exemplify areas in the prior art document(s) in which the examiner believed are the most relevant to the claimed subject matter. However, it is incumbent upon the applicant to analyze the prior art document(s) in its/their entirety since other areas of the document(s) may be relied upon at a later time to substantiate examiner's rationale of record. A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. W.L. Gore & associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984). However, "the prior art's mere disclosure of more than one alternative does not constitute a teaching away from any of these alternatives because such disclosure does not criticize, discredit, or otherwise discourage the solution claimed...." In re Fulton, 391 F.3d 1195, 1201, 73 USPQ2d 1141, 1146 (Fed. Cir. 2004).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kezhen Shen whose telephone number is (571) 270-1815. The examiner can normally be reached on Monday - Friday 7:30 am to 5:30 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vu Le can be reached on (571) 272-7332. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

ks

KIEU-OANH BUI
PRIMARY EXAMINER